

L9289.00121

09/701433

INTERNATIONAL APPLICATION NO.
PCT/JP00/01755INTERNATIONAL FILING DATE
March 23, 2000PRIORITY DATE CLAIMED
March 31, 1999

TITLE OF INVENTION

RADIO COMMUNICATION APPARATUS AND CODING PROCESSING METHOD

APPLICANT(S) FOR DO/EO/US

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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
 - a. is transmitted herewith (required only if not transmitted by the International Bureau).
 - b. has been transmitted by the International Bureau.
 - c. is not required, as the application was filed in the United States Receiving Office (RO/US).
6. A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. A copy of the International Search Report (PCT/ISA/210).
8. Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
 - a. are transmitted herewith (required only if not transmitted by the International Bureau).
 - b. have been transmitted by the International Bureau.
 - c. have not been made; however, the time limit for making such amendments has NOT expired.
 - d. have not been made and will not be made.
9. A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

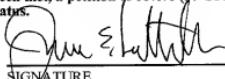
Items 13 to 20 below concern document(s) or information included:

13. An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. A **FIRST** preliminary amendment.
16. A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. A substitute specification.
18. A change of power of attorney and/or address letter.
19. Certificate of Mailing by Express Mail
20. Other items or information:

Claim for Priority with PCT/IB/304

PCT/IB/308

PCT/RO/101

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 09/701433	INTERNATIONAL APPLICATION NO. PCT/JP00/01755	ATTORNEY'S DOCKET NUMBER L9289.00121
21. The following fees are submitted:		CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) : <ul style="list-style-type: none"> <input type="checkbox"/> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO \$1,000.00 <input checked="" type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO \$860.00 <input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$710.00 <input type="checkbox"/> International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) \$690.00 <input type="checkbox"/> International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) \$100.00 		ENTER APPROPRIATE BASIC FEE AMOUNT = \$860.00
Surcharge of \$130.00 for furnishing the oath or declaration later than months from the earliest claimed priority date (37 CFR 1.492 (e)).		\$0.00
CLAIMS	NUMBER FILED	NUMBER EXTRA
Total claims	10 - 20 =	0
Independent claims	9 - 3 =	6
Multiple Dependent Claims (check if applicable).		<input type="checkbox"/>
TOTAL OF ABOVE CALCULATIONS =		\$1,340.00
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) (check if applicable).		<input type="checkbox"/> \$0.00
SUBTOTAL =		\$1,340.00
Processing fee of \$130.00 for furnishing the English translation later than months from the earliest claimed priority date (37 CFR 1.492 (f)).		<input type="checkbox"/> 20 <input type="checkbox"/> 30 + \$0.00
TOTAL NATIONAL FEE =		\$1,340.00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable).		<input checked="" type="checkbox"/> \$40.00
TOTAL FEES ENCLOSED =		\$1,380.00
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<input checked="" type="checkbox"/> A check in the amount of \$1,380.00 to cover the above fees is enclosed. <input type="checkbox"/> Please charge my Deposit Account No. 19-4375 in the amount of \$ to cover the above fees. A duplicate copy of this sheet is enclosed. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 19-4375 A duplicate copy of this sheet is enclosed.		
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.		
SEND ALL CORRESPONDENCE TO:		
James E. Ledbetter Stevens, Davis, Miller & Mosher, LLP 1615 L Street N.W., Suite 850 P.O. Box 34387 Washington, D.C. 20043-4387 Telephone: 202/408-5100 Faximile: 202/408-5200		
 SIGNATURE		
James E. Ledbetter NAME 28,732 REGISTRATION NUMBER November 29, 2000 DATE		

DESCRIPTION

RADIO COMMUNICATION APPARATUS AND CODING PROCESSING METHOD

5 Technical Field

The present invention relates to a radio communication apparatus and a coding processing method employed in mobile radio communication.

10 Background Art

In mobile radio communication, particularly in CDMA radio communication, Rate matching processing is performed in order to enhance an effect of error correction, and/or in order to transmit data such as a packet, ISDN and so forth while coupling the data. The Rate matching processing is repetition processing for increasing the number of bits of data in order to adjust coded data to frame length, or puncturing processing for reducing the number of bits of data in order to adjust coded data to frame length. For instance, in a transmitter side, in the case where the transmitter side causes the number of bits of data to be increased, in a receiver side, the receiver side is required to perform processing of decreasing of the number of bits of data.

In this case, since the transmitter side performs repetition, it is possible to increase a transmission power.

FIG. 1A is a block diagram illustrating a configuration of a conventional coding processing apparatus in the case where repetition is performed in a transmitter side. Also, FIG. 1B is a block diagram 5 illustrating a configuration of a conventional decoding processing apparatus in the case where repetition is performed in a transmitter side.

The coding processing apparatus 1 includes a coder 2, an error correction coder 3, a repetition section 3, 10 and an interleaving section 5. The decoding processing apparatus 10 includes a deinterleaving section 11, a puncturing section 12, an error correction decoder 13, and a decoder 14.

In the transmitter side, transmitted data 6 is coded 15 in the coder 2. This coded data is subjected to error correction coding processing such as convolutional coding and so forth in the error correction coder 3 before the number of bits is increased in the repetition section 4. The data after repetition is rearranged in the 20 interleaving section 5. Subsequently, the data is subjected to predetermined modulation processing and radio processing and so forth, before being transmitted from a transmission antenna 7.

On the other hand, in the receiver side, a signal 25 received by a reception antenna 15 is subjected to predetermined radio processing and demodulation processing and so forth before inverse rearrangement

against the interleaving is performed in the deinterleaving section 11. In this rearranged data, the number of bits which are increased in the transmitter side once are decreased in the puncturing section 12.

5 The data is subjected to error correction by Viterbi
decoding and so forth in the error correction decoder
13. This data after error correcting is decoded in the
decoder 14. According to the above processing, received
data 16 is obtained.

10 FIG. 2 is a view showing data arrangement in the
case where repetition is performed with the conventional
coding processing apparatus employed. Now, data
outputted from the coder 2 is taken to be {D1, D2, D3,
D4}. The data is subjected to error correction coding
15 processing with "code rate = 1/2" in the error correction
coder 3. As a result, in cases where D1 becomes d1 and
d2, D2 becomes d3 and d4, D3 becomes d5 and d6, and D4
becomes d7 and d8, data inputted to the repetition section
20 4 becomes data of 8 bits of {d1, d2, d3, d4, d5, d6, d7,
d8}. Further, the number of bits per 1 frame is set to
12 bits.

The repetition section 4 is provided with a Rate matching table. Further, a pattern of "0 and 1" is stored in the Rate matching table. The pattern of "0 and 1" causes a distribution of increase of bits within a frame to be even. Now, if the Rate matching table is taken to be {1, 0, 1, 0, 1, 0, 1, 0}, since bits corresponding

to "1" are increased, thus d1, d3, d5, and d7 showed by under lines are increased.

Accordingly, data after repetition becomes {d1, d1, d2, d3, d3, d4, d5, d5, d6, d7, d7, d8}. Careful 5 observation of the data after repetition reveals that there exist two increased bits and one not increased bit within continuous three bits, thus it is found that a distribution of increase of bits becomes even within a frame.

10 The data after repetition is subjected to interleaving in accordance with for instance an interleaving pattern ; $12[4[2 \times 2] \times 3[2 \times 2]]$. According to this processing, the data after interleaving becomes {d1, d5, d3, d7, d2, d6, d4, d8, d1, d5, d3, d7}.

15 According to these processing, it is possible to avoid a burst error in a propagation path in some degrees. Accordingly, it is possible to improve bit error rate characteristic in some degrees when the receiver side corrects errors.

20 However, in the above-described conventional coding processing apparatus, the increased bits caused by repetition are partial to a position within a frame according to an interleaving pattern. For this reason, an effect of the repetition deteriorates remarkably. 25 Consequently, the bit error rate characteristic deteriorates when the receiver side corrects errors.

Specifically, for instance, in an interleaving

pattern showed in FIG. 2, increased bits "d1, d3, d5, d7" are partial to both sides within the frame. Accordingly, in the case where a burst error occurs in a propagation path at portions with not-increased bits 5 "d2, d4, d6, d8", the bit error rate characteristic deteriorates when the receiver side corrects errors.

Disclosure of Invention

An object of the present invention is to provide 10 a radio communication apparatus and a coding processing method in which resistibility to a burst error in a propagation path is high, and the apparatus and method are capable of scheming improvement of communication quality.

15 The inventor of the present invention notes a cause why the increased bits due to the repetition are partial to a portion within a frame. In the case where the repetition is performed at a time about the whole data before interleaving, the increased bits due to the 20 repetition are partial to a portion within the frame. The inventor finds that the repetition is separated to be performed before and after interleaving in well-balanced condition, so that it is possible to prevent maldistribution of the increased bits due to the 25 repetition within the frame, and the inventor achieves the present invention.

Accordingly, in order to achieve the above-

described object, in the present invention, roughly half the number of bits increased due to the repetition are increased in accordance with a repetition before interleaving, while remaining the number of bits 5 increased due to the repetition are increased in accordance with a repetition after interleaving.

Brief Description of Drawings

FIG. 1A is a block diagram illustrating a configuration of a conventional coding processing 10 apparatus;

FIG. 1B is a block diagram illustrating a configuration of a conventional decoding processing apparatus;

FIG. 2 is a view showing data arrangement in the 15 case where repetition is performed with the conventional coding processing apparatus employed;

FIG. 3A is a block diagram illustrating a configuration of a coding processing apparatus according to an embodiment 1 of the present invention;

20 FIG. 3B is a block diagram illustrating a configuration of a decoding processing apparatus according to an embodiment 1 of the present invention;

FIG. 4 is a block diagram illustrating a configuration of a repetition section and a puncturing 25 section according to the embodiment 1 of the present invention;

FIG. 5 is a flowchart for explaining operation of

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a first repetition section according to the embodiment 1 of the present invention;

Fig. 6 is a flowchart for explaining operation of a second repetition section according to the embodiment 5 1 of the present invention;

FIG. 7 is a flowchart for explaining operation of a first puncturing section according to the embodiment 1 of the present invention;

FIG. 8 is a flowchart for explaining operation of 10 a second puncturing section according to the embodiment 1 of the present invention;

FIG. 9 is a view showing data arrangement in the case where repetition is performed with the coding processing apparatus employed according to the 15 embodiment 1 of the present invention;

FIG. 10A is a block diagram illustrating a configuration of a coding processing apparatus according to an embodiment 2 of the present invention;

FIG. 10B is a block diagram illustrating a 20 configuration of a decoding processing apparatus according to the embodiment 2 of the present invention;

FIG. 11A is a block diagram illustrating a configuration of a coding processing apparatus according to an embodiment 3 of the present invention; and

25 FIG. 11B is a block diagram illustrating a configuration of a decoding processing apparatus according to the embodiment 3 of the present invention.

Best Mode for Carrying Out the Invention

Embodiments of the present invention are explained in detail below with reference to accompanying drawings.

5 (Embodiment 1)

FIG. 3A is a block diagram illustrating a configuration of a coding processing apparatus according to the embodiment 1 of the present invention. Further,

FIG. 3B is a block diagram illustrating a configuration

10 of a decoding processing apparatus according to the embodiment 1 of the present invention. A coding processing apparatus 100 includes a coder 101, an error correction coder 102, a first repetition section 103, an interleaving section 104, and a second repetition section 105. In the meantime, a decoding processing apparatus 110 includes a first puncturing section 111, a deinterleaving section 112, a second puncturing section 113, an error correction decoder 114, and a decoder 115.

20 In the transmitter side, transmitted data 106 is coded in the coder 101. The coded data is subjected to error correction coding processing such as convolutional coding and so forth in the error correction coder 102, before being outputted to the first repetition section 103. The data after error correction coding processing is subjected to a first repetition as describe later in the first repetition section 103. The data after the

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first repetition is rearranged in the interleaving section 104, before being subjected to a second repetition as describe later in the second repetition section 105. The data after the second repetition is 5 subjected to predetermined modulation processing and predetermined radio processing and so forth thereafter. Then the data is transmitted from a transmission antenna 107.

On the other hand, in the receiver side, a signal 10 received by a reception antenna 116 is subjected to predetermined radio processing and predetermined demodulation processing and so forth. The data after predetermined radio processing and predetermined demodulation processing is subjected to a first 15 puncturing which is inverse processing against the second repetition in the first puncturing section 111. The data after the first puncturing is subjected to an inverse rearrangement against the interleaving in the transmitter side in the deinterleaving section 112. 20 This rearranged data is subjected to a second puncturing which is inverse processing against the first repetition in the second puncturing section 113. The data after the second puncturing is subjected to error correction by Viterbi decoding and so forth in the error correction 25 decoder 114, before being decoded in the decoder 115. According to the above processing, received data 117 is obtained.

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Next, there will be described about configuration of the first repetition section 103 while employing the block diagram illustrated in FIG. 4. In the first repetition section 103, an input memory 201 temporary stores therein data being subjected to error correction coding. A parameter storage section 202 stores therein various kinds of parameters necessary for performing repetition. A controller 203 outputs a control signal for performing read/write of data to a memory read/write section 204 on the basis of various kinds of parameters stored in the parameter storage section 202. The memory read/write section 204 reads the data from the input memory 201 successively, and outputs the data while increasing the number of bits to be targeted bits to an output memory 205 on the basis of the control signal. The output memory 205 stores the data outputted successively from the memory read/write section 204 up to the state where the data for one frame is completed. Then the output memory 205 outputs the data for one frame at the time when the data for one frame is completed.

Further, a configuration of the second repetition section 105 is roughly the same as that of the first repetition section 103. Accordingly, concerning the second repetition section 105, an explanation about the configuration is omitted. There will be explained about only operation in an operation explanation describe later. Furthermore, also configurations of the first

puncturing section 111 as well as the second puncturing section 113 are roughly the same as the configuration of the first repetition section 103. Accordingly, about the first puncturing section 111 as well as the second 5 puncturing section 113, an explanation about the configuration is omitted. There will be explained about only operation in an operation explanation as describe later.

Next, there will be explained about operation of 10 the first repetition section 103. FIG. 5 is a flowchart for explaining operation of the first repetition section 103. Firstly, in ST301, the controller 203 calculates increased the number of bits namely the total number of bits 'R' for repetition in accordance with an expression 15 (1) from the number of bits 'N' per one frame stored in the parameter storage section 202 and the number of bits 'NO' before repetition.

$$R = N - NO \quad (1)$$

Next, in ST302, the controller 203 calculates the 20 number of bits 'r1' for the first repetition. In order to perform repetition to the data while separating repetition into two stages in well-balanced condition, 'r1' is calculated in such a way of showing of an expression (2) with 'R' employed.

25 $r1 = R/2$ (rounding off less than a decimal point) (2)

Next, in ST303, the controller 203 calculates a

first repetition interval 'X1' that means whether the controller 203 performs the first repetition in every how many bits in accordance with an expression (3).

Next, in ST304, the controller 203 performs compensation of 'r1', and 'X1'. This compensation is one causing the first repetition to be executed in accordance with a code rate to be performed according to expressions (4) to (6). Specifically, for instance, in the case where a code rate of data is 1/2, the first repetition is performed in every the number of bits to be multiples of 2, while in the case where a code rate of data is 1/3, the first repetition is performed in every the number of bits to be multiples of 3. Thus 'r1' and 'X1' are compensated in accordance with above described manner.

Firstly, the controller 203 performs the remainder calculation showed in an expression (4).

$$\text{mod}(X_1 + m, C) = 0 \quad m \geq 0 \quad (4)$$

20 Here, 'C' is an inverse number of a code rate of data, and this expression (4) is one for calculating the minimum 'm' causing the remainder to be '0'(zero) when 'X1 + m' is divided by 'C'. The controller 203 calculates a compensated value 'X1'' of 'X1' in accordance with an expression (5) while employing 'm' calculated by this expression (4). According to this processing, 'X1' is compensated into 'X1''.

25

$$X1' = X1 + m \quad (5)$$

Further, the controller 203 calculates compensated value 'r1'' of 'r1' in accordance with an expression (6) while employing 'X1'' calculated by the expression (5).

5 According to this processing, 'r1' is compensated into 'r1''.

$$r1' = N0/X1' \text{ (rounding off less than decimal point)} \quad (6)$$

Subsequently, a value of a counter 'Ct' set in the 10 controller 203 is added one by one from '1' (one). Then, processing of ST305 to ST310 is performed repeatedly over 'N0' times up to the state where the value of the counter 'Ct' becomes 'N0'. In ST306, the controller 203 performs the remainder calculation of an expression (7).

15 $\text{mod}(Ct, X1') = b1 \quad (7)$

Here, 'b1' is a parameter for setting whether the first repetition is started from how many numbers of bits of a frame. The 'b1' is set in the parameter storage section 202 beforehand.

20 In ST306, in the case where the remainder of the division of dividing 'Ct' by 'X1'' becomes equal to 'b1', in ST307, the controller 203 sets the number of times 'n' of data output to '2'. in ST306, in the case where the remainder of the division of dividing 'Ct' by 'X1'' 25 does not become equal to 'b1', in ST308, the controller 203 sets the number of times 'n' of data output to '1'.

In ST309, the memory read/write section 204 reads

the data stored in the input memory 201 one bit by one bit to write to the output memory 205 over 'n' times. Namely, concerning the bit set to 'n=2', the number of bits is increased.

5 According to a processing-flow described-above, the first repetition of causing the number of bits to be increased for only the number of bits 'r1'' roughly half the number of total bits 'R' for the repetition is performed. Concerning the data after the first 10 repetition, rearrangement of data is performed in accordance with the interleaving pattern in the interleaving section 104, subsequently the data is subjected to the second repetition in the second repetition section 105.

15 Next, there will be described about operation of the second repetition section 105. FIG. 6 is a flowchart for explaining operation of the second repetition section 105.

Firstly, in ST401, the controller 203 within the second 20 repetition section 105 calculates the number of bits 'r2' for the second repetition in accordance with an expression (8) from the number of total bits 'R' for the repetition calculated by the first repetition section 103 and compensated number of bits 'r1'' for the first 25 repetition.

$$r2 = R - r1' \quad (8)$$

Next, in ST402, the controller 203 calculates a

second repetition interval 'X2' that means whether the controller 203 performs the second repetition in every how many bits in accordance with an expression (9).

Here, 'N1' is 'N1 = N0 + r1', which represents the number of bits after the first repetition.

Subsequently, a value of the counter 'Ct' set in the controller 203 is added one by one from '1'(one).

10 Then, processing of ST403 to ST408 is performed repeatedly over 'N1' times up to the state where the value of the counter 'Ct' becomes 'N1'. In ST404, the controller 203 performs the remainder calculation of an expression (10).

$$15 \quad \text{mod}(Ct, \ x2) = b2 \quad (10)$$

Here, 'b2' is a parameter for setting whether the second repetition is started from how many numbers of bits of a frame. This 'b2' is set in the parameter storage section 202 beforehand.

20 In ST404, in the case where the remainder of the division of dividing 'Ct' by 'X2' becomes equal to 'b2', in ST405, the controller 203 sets the number of times 'n' of data output to '2'. While, in ST404, in the case where the remainder of the division of dividing 'Ct' by
25 'X2' does not become equal to 'b2', in ST406, the controller 203 sets the number of times 'n' of data output to '1'.

In ST407, the memory read/write section 204 reads the data stored in the input memory 201 one bit by one bit to write to the output memory 205 over 'n' times. Namely, concerning the bit set to 'n=2', the number of 5 bits is increased.

According to the processing-flow described-above, the second repetition is performed to the data after the first repetition. According to this processing, a repetition satisfying the total number of bits per one 10 frame is performed.

Next, there will be described concerning processing of the receiver side. In the receiver side, the first puncturing section 111 and the second puncturing section 113 perform inverse processing against the transmitter 15 side, namely perform puncturing, to the bits increased by the first repetition and the second repetition in the transmitter side. According to this processing, received data 117 is obtained. Specific operation is as follows.

Firstly, there will be described about operation 20 of the first puncturing section 111. FIG. 7 is a flowchart for explaining operation of the first puncturing section 111. The first puncturing section 111 performs processing for decreasing the bits increased in the second repetition section 105.

25 In ST501, a first puncturing interval 'X2' that means whether the first puncturing is performed in every how many bits is set to the parameter storage section

202 in accordance with control data transmitted from the transmitter side. This 'X2' is equal to the second repetition interval 'X2'.

Subsequently, the processing of ST502 to ST505 is 5 performed repeatedly over 'N' times up to the state where a value of the counter 'Ct' set in the controller 203 is added one by one from '1'(one) to come into 'N'. Here, 'N' is 'N = N0 + r1' + r2', thus representing the number of bits after the second repetition, namely representing 10 the number of bits per one frame. In ST503, the controller 203 performs the remainder calculation of an expression (11).

$$\text{mod}(Ct, X2) = b2 \quad (11)$$

Here, 'b2' is equal to 'b2' which is employed when 15 the second repetition is performed. The 'b2' is set to the parameter storage section 202 in accordance with the above control signal.

Next, in ST504, the memory read/write section 204 reads data stored in the input memory 201 one bit by one 20 bit. Then, in the case where the remainder of the division of dividing 'Ct' by 'X2' does not become equal to 'b2', the memory read/write section 204 writes the read data to the output memory 205 once. While in the case where the remainder of the division of dividing 'Ct' 25 by 'X2' becomes equal to 'b2', the memory read/write section 204 abolishes the read data.

According to the processing-flow described-above,

the first puncturing is performed to the bits increased by the second repetition. Concerning the data after the first puncturing, an inverse rearrangement against the rearrangement of data performed in the interleaving section 104 is performed in the deinterleaving section 112. Subsequently, the data is subjected to the second puncturing in the second puncturing section 113.

Next, there will be described operation of the second puncturing section 113. FIG. 8 is a flowchart for explaining operation of the second puncturing section 113. The second puncturing section 113 performs processing for decreasing the bits increased by the first repetition section 103.

Firstly, in ST601, a second puncturing interval 'X1'' that means whether the second puncturing is performed in every how many bits is set to the parameter storage section 202 in accordance with the above control data. This 'X1'' is equal to the compensated first repetition interval 'X1''.

Subsequently, the processing of ST602 to ST605 is performed repeatedly over 'N1' times up to the state where a value of the counter 'Ct' set in the controller 203 is added one by one from '1' (one) to come into 'N1'. This 'N1' is equal to 'N1' which is employed in the second repetition to be set to the controller 203 in accordance with the above control signal.

In ST603, the controller 203 performs the remainder

calculation of an expression (12).

$$\text{mod}(\text{ct}, \text{x1}') = \text{bl} \quad (12)$$

Here, 'b1' is equal to the 'b1' employed when the first repetition is performed, to be set to the parameter 5 storage section 202 in accordance with the above control signal.

Next, in ST604, the memory read/write section 204 reads the data stored in the input memory 201 one bit by one bit. Then in the case where the remainder of the division of dividing 'Ct' by 'X1' does not become equal to 'b1', the memory read/write section 204 writes the read data to the output memory 205 once. While in the case where the remainder of the division of dividing 'Ct' by 'X1' becomes equal to 'b2', the memory read/write section 204 abolishes the read data.

According to the processing-flow described-above, the second puncturing is performed to the bits increased by the first repetition. The data after the second puncturing is subjected to error correction by Viterbi decoding and so forth in the error correction decoder 114, before being decoded in the decoder 115. According to this processing, received data 117 is obtained.

Next, there will be described the circumstances in detail in which transmitted data is subjected to repetition and interleaving due to the coding processing apparatus 100 of the present embodiment while employing

Now, data outputted from the coder 101 is taken to be {D1, D2, D3, D4}. The data is subjected to error correction coding processing with "code rate = 1/2" in the error correction coder 102. As a result, in cases 5 where 'D1' becomes 'd1', and 'd2', 'D2' becomes 'd3', and 'd4', 'D3' becomes 'd5', and 'd6', and 'D4' becomes 'd7', and 'd8', data inputted to the first repetition section 103 becomes data of 8 bits of {d1, d2, d3, d4, d5, d6, d7, d8}. Further, the number of bits per one 10 frame is 12 bits.

In the first place, the first repetition section 103 performs the first repetition in accordance with processing-flow of FIG. 5. Firstly, in ST301 to ST303, 'R', 'r1', and 'X1' are calculated in accordance with 15 above expressions (1) to (3). Following result is obtained.

$$R = N - N_0 = 12 - 8 = 4 \quad (13)$$

$$r_1 = R/2 = 4/2 = 2 \quad (14)$$

$$X_1 = N_0/r_1 = 8/2 = 4 \quad (15)$$

20 Next, in ST304, 'r1' and 'X1' are compensated in accordance with above expressions (4) to (6). Now, since the code rate of the error correction coding processing is '1/2', 'C' becomes 'C=2'. Consequently, above expression (4) is calculated as following way.

$$\begin{aligned} 25 \quad \text{mod}(X_1 + m, C) &= 0 \\ \text{mod}(4 + m, 2) &= 0 \\ \therefore m &= 0 \quad (16) \end{aligned}$$

Here, since 'm' is 'm=0', following result is obtained in accordance with above expressions (5), and (6).

$$x_1' = x_1 = 4 \quad (17)$$

5 $r_1' = r_1 = 2 \quad (18)$

Next, in ST305 to ST310, the number of bits of corresponding bits is increased in accordance with the above expression (7) up to the state where 'Ct' becomes 'NO' from '1'. Now, in the case where 'b1' is set to 10 "b1=2", in accordance with the above expression (7), the number of bits of 'd2' to be data of the second bit as well as the number of bits of 'd6' to be data of the sixth bit are increased, thus the first repetition is performed. Consequently, the data after the first repetition 15 becomes {d1, d2, d2, d3, d4, d5, d6, d6, d7, d8} as showed in FIG. 9. Further, the data showed by underline in FIG. 9 are ones whose number of bits is increased due to repetition.

Next, concerning the data after the first 20 repetition, rearrangement of data is performed in accordance with interleaving pattern "10[5[3x2]x2]" in the interleaving section 104. As a result, the data after interleaving becomes {d1, d4, d7, d2, d6, d2, d5, d8, d3, d6}.

25 Next, the second repetition section 105 performs the second repetition to the data after interleaving in accordance with the processing-flow of FIG. 6. Firstly,

in ST401 to ST402, in accordance with the above expressions (8) to (9), 'r2' and 'X2' are calculated as follows:

$$r2 = R - r1' = 4 - 2 = 2 \quad (19)$$

5 $X2 = N1/r2 = 10/2 = 5 \quad (20)$

Next, in ST403 to ST408, the number of bits of corresponding bits is increased in accordance with the above expression (10) up to the state where 'Ct' becomes 'N1' from '1'. Now, in the case where 'b2' is set to 10 'b2=2', in accordance with the above expression (10), the number of bits of 'd4' to be data of the second bit as well as the number of bits of 'd5' to be data of the seventh bit are increased, thus the second repetition is performed. Consequently, the data after the second 15 repetition becomes {d1, d4, d4, d7, d2, d6, d2, d5, d5, d8, d3, d6} as showed in FIG. 9.

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since repetition is performed at two stages 20 before and after interleaving, it is possible to prevent that the bits increased due to repetition exist while being partial to one position within a frame. For that reason, it is possible to improve a bit error rate characteristic when the receiver side performs error 25 correction in comparison with the conventional coding processing apparatus and the conventional decoding processing apparatus in which repetition is performed

only once before interleaving.

Further, in the above specific example, in the case where the interleaving pattern is $10[5[3 \times 2] \times 2]$, an effect of the present embodiment becomes the most remarkable. However, even though an interleaving pattern is another one, it can be observed that the present embodiment has an effect.

Furthermore, in the above specific example, there is described the embodiment while setting various kinds of parameters arbitrarily. However, it is nothing but one example. Accordingly, the effect of the present embodiment is not observed while being limited from values of these parameters, but the effect of the present embodiment is observed even though parameters adopt another values.

(Embodiment 2)

Next, there will be described an embodiment 2 of the present invention. FIG. 10A is a block diagram illustrating a configuration of a coding processing apparatus according to the embodiment 2 of the present invention. Further, FIG. 10B is a block diagram illustrating a configuration of a decoding processing apparatus according to the embodiment 2 of the present invention. In a coding processing apparatus 800, the configuration of the coding processing apparatus 800 is one in which the second repetition section 105 is removed.

from the coding processing apparatus 100 of the embodiment 1. Another configuration and operation of respective sections are the same as that of coding processing apparatus 100.

5 Consequently, in a transmitter side, the data which is subjected to the error correction coding processing in the error correction coder 102 is subjected to a first repetition by the first repetition section 103 in which 'r1' calculated in ST302 at the processing-flow showed
10 in FIG. 5 described-above is taken to be ' $r1=R$ '. The data after the first repetition is rearranged in the interleaving section 104. Subsequently, the data is subjected to predetermined modulation processing and predetermined radio processing and so forth, before
15 being transmitted from the transmission antenna 107.

On the other hand, in a decoding processing apparatus 810, the configuration of the decoding processing apparatus 810 is one in which the first puncturing section 111 is removed from the decoding processing apparatus 110 of the embodiment 1. Another configuration and operation of respective sections are the same as that of decoding processing apparatus 110.

Consequently, in the receiver side, data to which inverse rearrangement against the interleaving of the transmitter side is performed in the deinterleaving section 112 is subjected to inverse second puncturing against the first repetition in accordance with the

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processing-flow showed in FIG. 8 described above by the second puncturing section 113. The data after the second puncturing is subjected to the error correction by Viterbi decoding and so forth in the error correction 5 decoder 114.

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, the repetition is performed while determining increased bits in accordance with the code 10 rate such that in the case where the code rate of the data is '1/2', the increased bits are determined in every the number of bits of multiples of 2, and such that in the case where the code rate of the data is '1/3', the increased bits are determined in every the number of bits 15 of multiples of 3. Consequently, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, it is possible to prevent that the repetition is performed repeatedly to a plurality of data after error correction coding, which 20 are generated from the same data before error correction coding, caused by error correction coding processing. Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since it is possible to enhance an effect 25 of the error correction coding, it is possible to improve a bit error rate characteristic when the receiver side performs error correction in comparison with the

conventional coding processing apparatus and the conventional decoding processing apparatus.

(Embodiment 3)

5 Next, there will be described an embodiment 3 of
the present invention. FIG. 11A is a block diagram
illustrating a configuration of a coding processing
apparatus according to an embodiment 3 of the present
invention. Further, FIG. 11B is a block diagram
10 illustrating a configuration of a decoding processing
apparatus according to the embodiment 3 of the present
invention.

In a coding processing apparatus 900, the configuration of the coding processing apparatus is one in which the first repetition section 103 is removed from the coding processing apparatus 100 of the first embodiment. Another configuration and operation of respective sections are the same as that of the coding processing apparatus 100.

20 Consequently, in the transmitter side, the data
which is rearranged in the interleaving section 104 is
subjected to a second repetition by the second repetition
section 105 in which 'r2' calculated in ST401 at the
processing flow showed in FIG. 6 described-above is taken
25 to be 'r2=R'. The data after the second repetition is
subjected to predetermined modulation processing and
predetermined radio processing and so forth, before

being transmitted from the transmission antenna 107.

On the other hand, in a decoding processing apparatus 910, the configuration is one in which the second puncturing section 113 is removed from the decoding processing apparatus 110 of the embodiment 1. Another configuration and operation of respective sections are the same as that of the decoding-coding processing apparatus 110.

Consequently, in the receiver side, a signal received by the reception antenna 116 is subjected to predetermined radio processing and predetermined demodulation processing and so forth. Subsequently, the received signal is subjected to a first puncturing which is inverse processing against the second repetition in accordance with the processing-flow showed in FIG. 7 described-above by the first puncturing section 111. Concerning the data after the first puncturing, inverse rearrangement against the interleaving of the transmitter side is performed in the deinterleaving section 112.

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since the repetition is performed after interleaving, it is possible to prevent that the bits increased due to repetition exist while being partial to one position within a frame. Consequently, according to the coding processing apparatus and the decoding

processing apparatus of the present embodiment, it is possible to improve a bit error rate characteristic when the receiver side performs error correction in comparison with the conventional coding processing apparatus and the conventional decoding processing apparatus in which repetition is performed before interleaving.

The coding processing apparatus and the decoding processing apparatus according to the embodiments 1 to 3 described-above are applicable to a base station apparatus employed in a radio communication system, and applicable to a communication terminal apparatus such as a mobile station for performing radio communication to this base station apparatus. In the case of application, since the base station apparatus and the communication terminal apparatus are mounted with the coding processing apparatus and the decoding processing apparatus, which can lower the bit error rate, it is possible to scheme improvement of communication quality.

20 Further, in the explanation of the above
embodiments 1 to 3, for the sake of convenience, there
is explained the embodiments while separating the
apparatus of the present invention into the transmitter
and the receiver. However, a radio communication
25 apparatus in a CDMA radio communication system also can
be provided with both of the transmitter and the receiver.

As described above, according to the present

invention, it is possible to scheme improvement of communication quality because resistibility to a burst error in a propagation path becomes high.

This application is based on the Japanese Patent 5 Application No. HEI11-092078 filed on March 31, 1999, entire content of which is expressly incorporated by reference herein.

Industrial Applicability

10 The present invention is applicable to a base station apparatus employed in a radio communication system and/or a communication terminal apparatus such as a mobile station performing radio communication between the base station apparatus and the mobile 15 station.

CLAIMS

1. A radio communication apparatus comprising:
a first number-of-bits increaser for increasing the
specified number of bits among the number of bits for
5 a Rate matching in data subjected to error correction
coding;
an interleaver for rearranging data whose the
number of bits is increased; and
a second number-of-bits increaser for increasing
10 remaining the number of bits among the number of bits
for the Rate matching in rearranged data.
2. A radio communication apparatus according to
claim 1, wherein the first number-of-bits increaser
increases the number of bits of the data that is subjected
15 to the error correction coding in accordance with error
correction code rate.
3. A radio communication apparatus comprising:
a number-of-bits increaser for increasing the
number of bits of data that is subjected to error
20 correction coding in accordance with error correction
code rate; and
an interleaver for rearranging data whose the
number of bits is increased.
4. A radio communication apparatus comprising:
25 a receiver for receiving data whose the number of
bits is increased before and after an interleaving;
a first number-of-bits decreaser for decreasing the

number of bits increased after the interleaving in received data;

5 a deinterleaver for performing inverse rearrangement against the interleaving in data whose the number of bits is decreased; and

a second number-of-bits decreaser for decreasing the number of bits increased before the interleaving in data which is subjected to a deinterleaving.

10 5. A radio communication apparatus comprising:
a receiver for receiving data whose the number of bits is increased in accordance with error correction code rate before the data is rearranged;

15 a deinterleaver for performing inverse rearrangement against an interleaving in received data; and

a number-of-bits decreaser for decreasing the number of bits in data that is subjected to a deinterleaving.

20 6. A communication terminal apparatus mounted with a radio communication apparatus, the radio communication apparatus comprising:

25 a first number-of-bits increaser for increasing the specified number of bits among the number of bits for a Rate matching in data subjected to error correction coding;

an interleaver for rearranging data whose the number of bits is increased; and

a second number-of-bits increaser for increasing remaining the number of bits among the number of bits for the Rate matching in rearranged data.

7. A communication terminal apparatus mounted 5 with a radio communication apparatus, the radio communication apparatus comprising:

a receiver for receiving data whose the number of bits is increased before and after an interleaving;

10 a first number-of-bits decreaser for decreasing the number of bits increased after the interleaving in received data;

a deinterleaver for performing inverse rearrangement against the interleaving in data whose the number of bits is decreased; and

15 a second number-of-bits decreaser for decreasing the number of bits increased before the interleaving in data which is subjected to a deinterleaving.

8. A base station apparatus mounted with a radio communication apparatus, the radio communication 20 apparatus comprising:

a first number-of-bits increaser for increasing the specified number of bits among the number of bits for a Rate matching in data subjected to error correction coding;

25 an interleaver for rearranging data whose the number of bits is increased; and

a second number-of-bits increaser for increasing

remaining the number of bits among the number of bits for the Rate matching in rearranged data.

9. A base station apparatus mounted with a radio communication apparatus comprising:

5 a receiver for receiving data whose the number of bits is increased before and after an interleaving;

a first number-of-bits decreaser for decreasing the number of bits increased after the interleaving in received data;

10 a deinterleaver for performing inverse rearrangement against the interleaving in data whose the number of bits is decreased; and

a second number-of-bits decreaser for decreasing the number of bits increased before the interleaving in data which is subjected to a deinterleaving.

10. A coding processing method comprising:

increasing the specified number of bits among the number of bits for a Rate matching in data subjected to error correction coding;

20 rearranging data whose the number of bits is increased; and

increasing remaining the number of bits among the number of bits for the Rate matching in rearranged data.

ABSTRACT

In a coding processing apparatus, a first repetition section increases the number of bits of data about roughly half the number of bits among the number 5 of bits increased by a repetition. An interleaving section performs rearrangement of data whose the number of bits is increased. A second repetition section increases the number of bits of rearranged data about remaining the number of bits increased by the repetition.

10

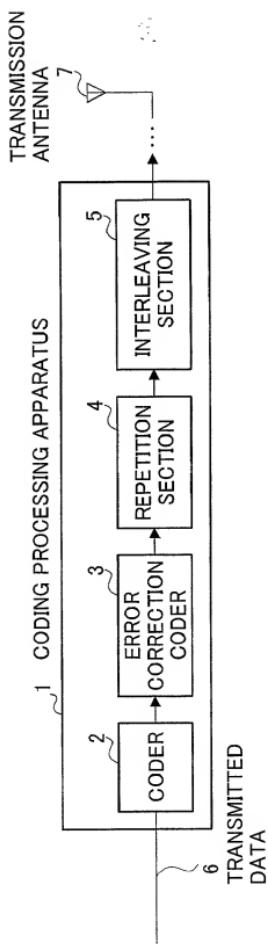


FIG. 1A

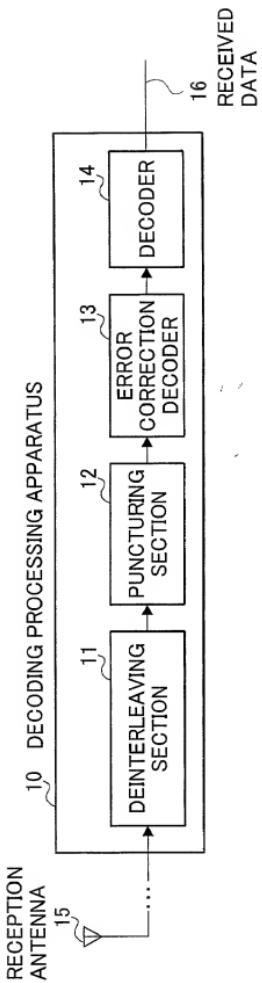


FIG. 1B

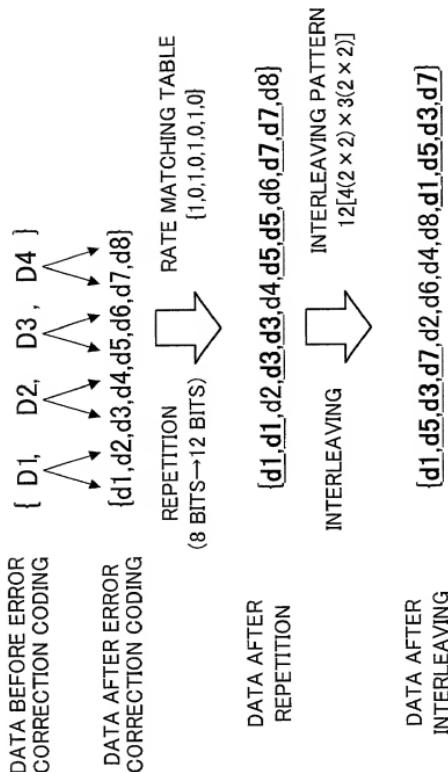


FIG.2

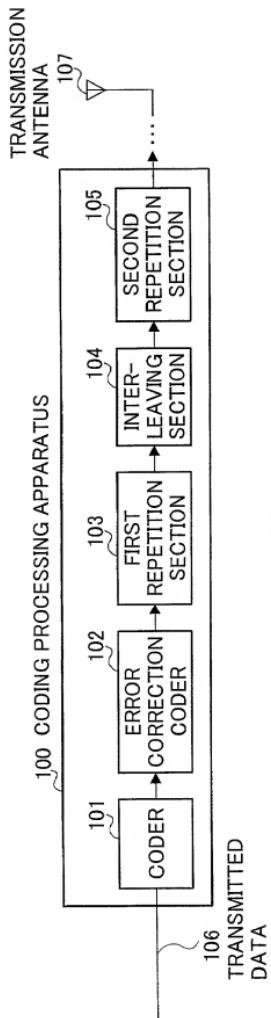


FIG.3A

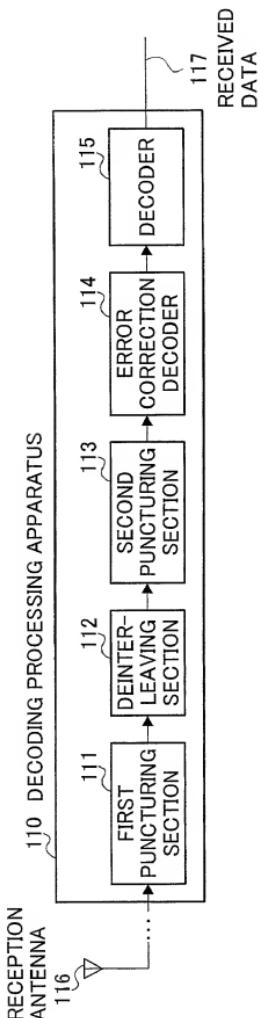


FIG.3B

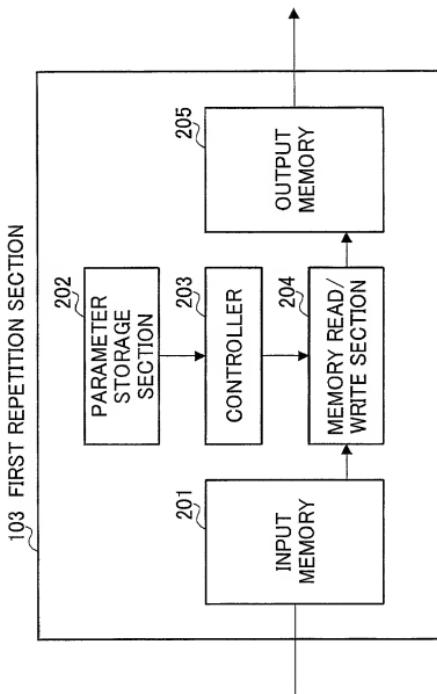


FIG.4

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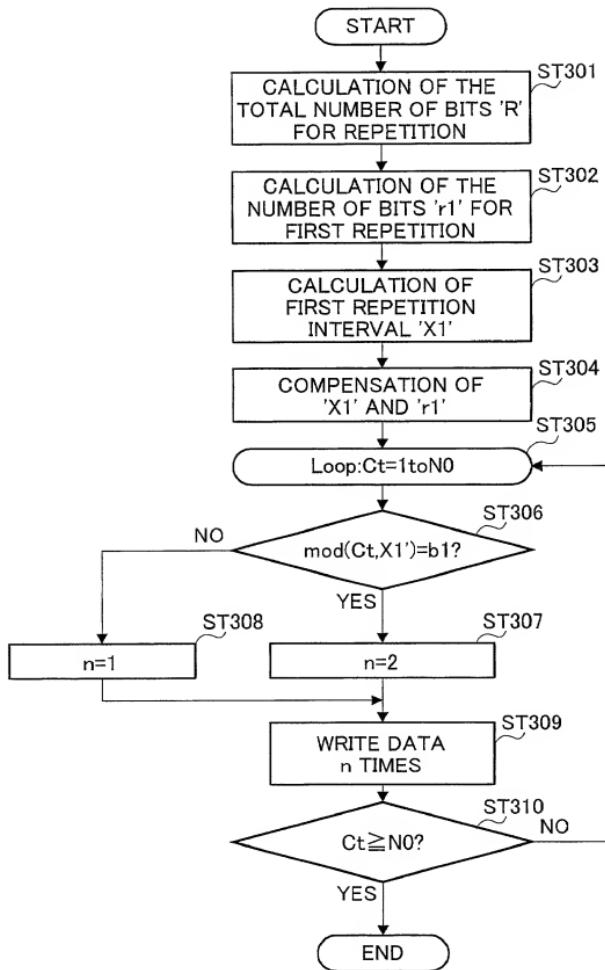


FIG.5

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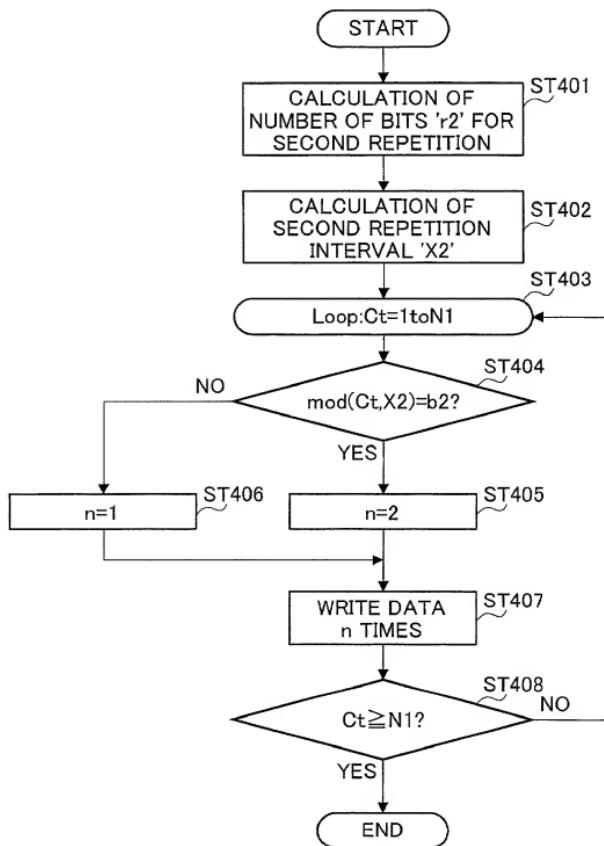


FIG.6

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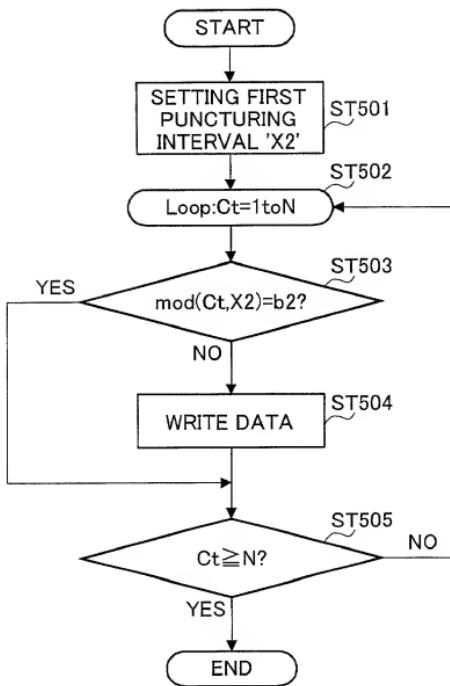


FIG.7

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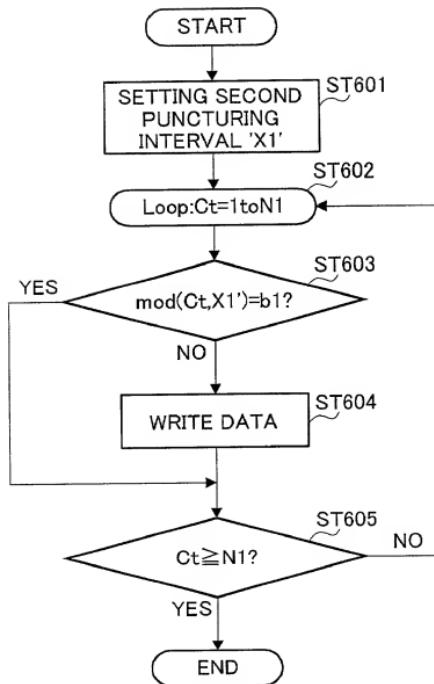


FIG.8

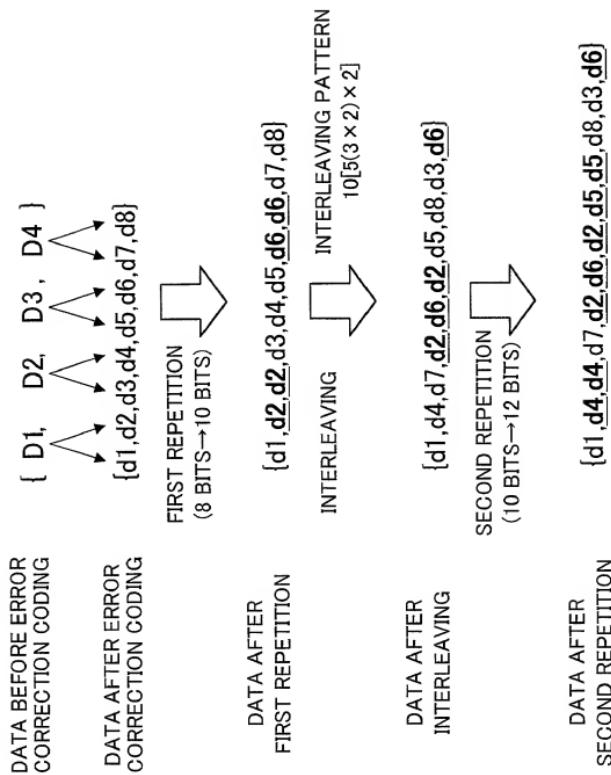


FIG.9

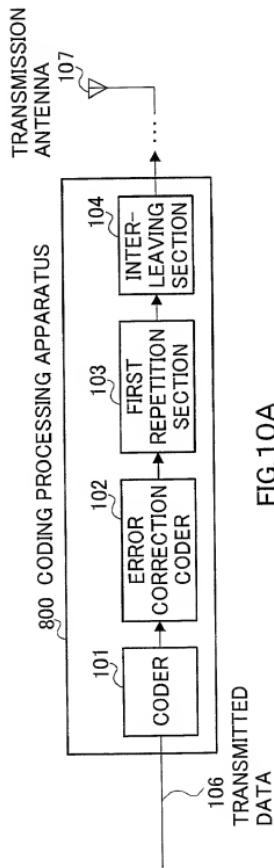


FIG. 10A

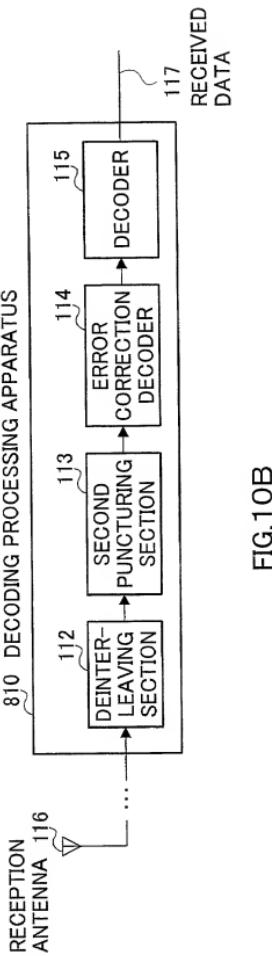


FIG. 10B

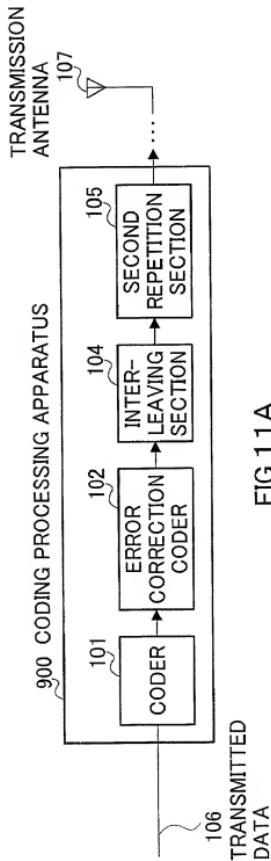


FIG. 11A

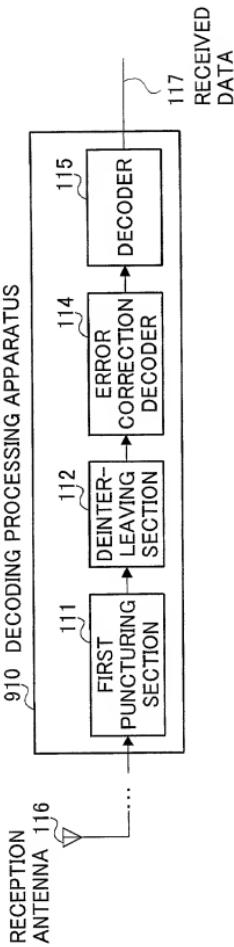


FIG. 11B

APPLICATION FOR UNITED STATES PATENT
Declaration for Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on

the invention entitled: **RADIO COMMUNICATION APPARATUS AND CODING PROCESSING METHOD**

the specification of which 2 (file no. _____)

I hereby declare that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended, by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me which is material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application (s) for patent or inventor's certificate listed below and also have identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date earlier than that of the application(s) on which priority is claimed.

Prior (Foreign) Application(s) any Priority Claims Under 35 U.S.C. 119			Priority Claimed
12a (Country)	(Number)	(Day/Month/Year Filed)	[] Yes [] No
(Country)	(Number)	(Day/Month/Year Filed)	[] Yes [] No
Priority Claim(s) from U.S. Provisional Application(s) – I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:			

12b	Application No.	Day/Month/Year Filed	Application No.	Day/Month/Year Filed
<p>Do not use this portion to identify a PCT application if the prior application is to the U.S. National phase of the PCT application</p> <p>I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below, and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between filing date of the prior application and the national or PCT international filing date of this application.</p>				
13	(U.S. Application Number)	(U.S. Filing Date)	Status (patented, pending, abandoned)	

I hereby appoint the following attorneys of the firm of Stevens, Davis, Miller & Mosher, L.L.P. as my attorneys of record with full power of substitution and revocation to prosecute this application and to transact all business in the Patent and Trademark Office:

3 James E. Ledbetter, Reg. No. 28732; Thomas P. Pavelko, Reg. No. 31689; and Anthony P. Venturino, Reg. No. 31674.

ALL CORRESPONDENCE IN CONNECTION WITH THIS APPLICATION SHOULD BE SENT TO STEVENS, DAVIS, MILLER & MOSHER, L.L.P., 1615 L Street, N.W., Suite 850, Washington, D.C. 20036, TELEPHONE (202) 408-5100. FACSIMILE (202) 408-5200.

See page 2 for signature lines

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

PAGE 2 OF U.S.A. DECLARATION FORM

14a	Typewritten Full Name of Sole or First Inventor	1/10 <u>Kuniyuki</u> Given Name Middle Name KAJITA Family Name		
15a	Inventor's Signature	<u>Kuniyuki</u> <u>Kajita</u>		
16a	Date of Signature	Month	Day	Year
17a	Residence	Yokosuka-shi	Kanagawa	JAPAN
18a	Citizenship	JAPAN		
19a	Post Office Address (Insert complete mailing address, including country)	6-2-807, Hikari no Oka, Yokosuka-shi, Kanagawa 239-0847 JAPAN		
14b	Typewritten Full Name of Sole or First Inventor	Given Name Middle Name Family Name		
15b	Inventor's Signature			
16b	Date of Signature	Month	Day	Year
17b	Residence	City	State or Province	Country
18b	Citizenship			
19b	Post Office Address (Insert complete mailing address, including country)			
14c	Typewritten Full Name of Sole or First Inventor	Given Name Middle Name Family Name		
15c	Inventor's Signature			
16c	Date of Signature	Month	Day	Year
17c	Residence	City	State or Province	Country
18c	Citizenship			
19c	Post Office Address (Insert complete mailing address, including country)			
14d	Typewritten Full Name of Sole or First Inventor	Given Name Middle Name Family Name		
15d	Inventor's Signature			
16d	Date of Signature	Month	Day	Year
17d	Residence	City	State or Province	Country
18d	Citizenship			
19d	Post Office Address (Insert complete mailing address, including country)			

*Note to Inventor: Please sign name on line 15 exactly as it appears in line 14 and insert the actual date of signing on line 16. If there are more than four inventors, please add a copy of this page for identification and signatures for the additional inventors.